A MONOLITHIC DOUBLE BALANCED SINGLE SIDEBAND MODULATOR

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ABSTRACT

A novel approach to single sideband modulation is presented which employs two differential FET pairs to obtain carrier and undesired sideband cancellation throughout a broad frequency range. This double balanced structure is also space thrifty and contains only MESFETS as active elements, thus lending itself to a monolithic implementation.

INTRODUCTION

Single sideband modulators have numerous applications in a variety of new communication and EW systems. Recent improvements in baseband to baseband translation techniques have generated new applications for single sideband modulators in spectrum efficient communication systems. The single sideband modulator in SSB AM analog transmission provides a substantial savings in bandwidth over FM systems. Recently, single sideband modulators have found applications in ECM jammers and decoys where the modulator is used to impart a low frequency shift in the received radar frequency. This frequency shift simulates a Doppler offset, representing a velocity delta between the tracking radar and the receiver/transmitter. Sweeping the frequency offset through several hundred or thousand Hertz passes the simulated radar return through the velocity gate of the tracking radar, effectively "fooling" the radar. The technique may also be used in a solid state replacement of serrodyned tube transmitters. The single sideband offset of the modulator simulates the transit time modulation of the carrier by a serrodyne (saw tooth) modulating voltage on the electron gun of the tube.

Conventional vector modulator or dual mixer approaches to single sideband modulation are inappropriate for new monolithic, integrated systems. Vector modulators require large wavelength dependent structures such as switched lines or loaded lines. Thus a large portion of the monolithic GaAs substrate upon which the vector modulator is integrated will simply be an expensive passive substrate for transmission lines. The dual mixer approach requires three baluns (for double balanced performance) and wavelength dependent matching networks, thus it too is inappropriate for integration on a monolithic substrate.

The technique to be presented is a novel implementation which uses GaAs MESFETs as nonlinear elements rather than diodes. The approach requires no wavelength dependent baluns because the arrangement of FETs into differential pairs provides balance. The bandwidth of the structure is essentially limited by the matching networks. The primary advantage of the approach is its small size which lends itself to monolithic integration.

Small signal models of the mixer were constructed using measured FET small signal parameters to predict input and output impedances and stability. However, in order to estimate the actual performance of the mixer (in terms of conversion loss, carrier and sideband suppression) nonlinear models were constructed on PSPICE. A simple prototype monolithic modulator was fabricated and the models were used to verify performance as a function of bias conditions and input signal levels.

APPROACH

The approach, shown in Figure 1, operates in essentially the same manner as conventional single sideband or image reject mixers. Undesired mixing products are suppressed by properly phasing the R.F. and modulating signals. The equation for single sideband modulation in the time domain is:

$$x_c(t) = \tfrac{1}{2} A_c [\, x(t) \cos w_c t \mp \hat{x}(t) \sin w_c t \,]$$

where $w_c t$ is the carrier frequency, $x(t)$ is the modulating waveform and $\hat{x}(t)$ is the Hilbert transform of $x(t)$. (physically, $\hat{x}(t)$ is simply $x(t)$ with its frequency components shifted by -90 degrees, or in quadrature). $x_c(t)$ is the signal summed at the output of the mixer.

If $x(t)$ is a tone modulation, for example $x(t) = A_m \cos(w_m t)$, then $x(t)$ is the in-phase (I) modulation and $\hat{x}(t)$ is the quadrature (Q) modulation. The above equation reduces to:

$$x_c(t) = \tfrac{1}{2} A_m A_c \cos(w_c \pm w_m)t$$

Thus this single sideband modulator, as a conventional modulator, relies on the quadrature phase relationship of the R.F. and LO signal to cancel the undesired sideband. For carrier rejection, however, the approach relies on the balance between the FETs in the differential pairs,

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rather than mixer diode and balun balance. The design provides isolation between all three ports as a result of the double balanced geometry and unilateral gain of the FETs.

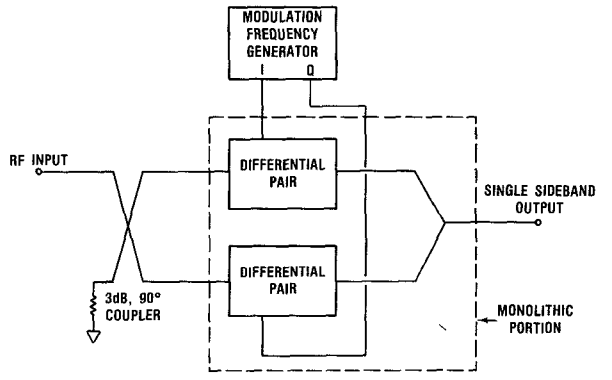

Figure 1. Schematic of Single Sideband Modulator and Coupler

The approach schematic is shown in Figure 2 The circuit consists of two differential FET pairs. The common source node of each pair is biased through a third FET, which acts as a constant current source. The drain node of each pair is summed in phase. The modulator requires the application of a quadrature carrier R.F signal to the gate of one FET in each pair. This quadrature split is provided by a Lange coupler. The modulation frequency (or audio offset) is split in quadrature (I and Q), and applied to the gate of the second FET in each pair. The constant current source attached to the common source node provides an R.F. sensing voltage for the second FET on the opposing side of the pair, forcing the R.F. current through this FET to oppose the R.F. current through the first FET. Similarly, opposing or out-of-phase currents exist in the two FETs for the modulation frequency. Thus, these signal currents will cancel in the source node, and consequently, in the drain node of the FET pair.

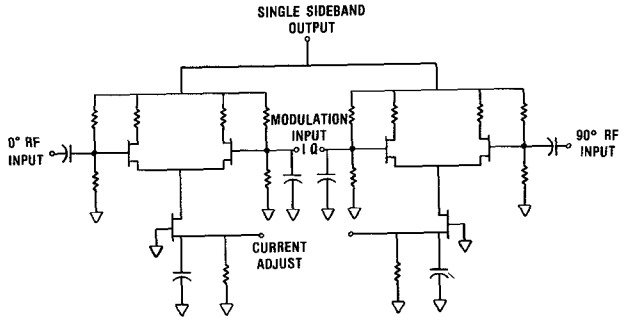

Figure 2. Double Balanced Single Sideband Modulator Circuit

The nonlinear mixing of the currents creates harmonic currents in the drain and source networks of the differential pair. These currents are the products of the in-phase R.F. and the out-of-phase audio (modulation) in the first FET, and the out-of-phase R.F. and in-phase audio in the second FET. Thus, the products of the currents resulting from mixing are in-phase in the source and in the drain nodes. The result is a double sideband spectrum in the drain where the carrier and modulation currents cancel and the product currents add constructively. The double sideband spectrum from each differential pair is summed, and as a result of the relative phase of sidebands provided by the quadrature R.F. and audio signals, the lower sidebands cancel and the upper sidebands combine. If the I and Q inputs are reversed in phase, the lower sidebands combine and the upper sidebands cancel.

The R.F. and modulation signals manifest themselves as difference mode inputs, thus carrier suppression is strongly a function of the match between the FET pairs. The products tend to add because they manifest themselves as common mode inputs. The in-phase products modulate a current in the non-ideal current source, producing a voltage in the drain network. Thus the conversion efficiency depends partially on common mode gain.

PERFORMANCE

The performance of the modulator depends on several factors. Carrier suppression will require tightly matched devices within the differential pair for balanced operation. Undesired sideband cancellation is a function of device matching between differential pairs, including the constant current sources, and the quality of quadrature in both the R.F. and audio signals The monolithic approach is uniquely appropriate for providing several desirable characteristics for undesired product suppression. The proximity of devices on the monolithic substrate will improve uniformity, thus providing well matched FET pairs. Conversion loss depends on the efficiency of the mixing process within the differential pair, which is a combination of the commutative switching of the applied audio offset frequency and the nonlinear generation of spectral products. The bandwidth of the modulator is restricted by the bandwidth of the input and output impedance matching networks, and the bandwidth of the coupler which provides the quadrature R.F. signal.

A prototype monolithic modulator has been designed, processed and tested at Texas Instruments (Figure 3). The FETs are 150 μm devices with one micron gates. The circuit is self biased with bypass capacitors and bias resistors integrated on the chip. The monolithic modulator is mounted on a thin film network (TFN) with a hybrid Lange Coupler and biased such that the DC voltage on the gates of the differential pairs is approximately half the applied drain voltage. The drain voltage is 6V and the current source is at approximately 50% I_{dss}.

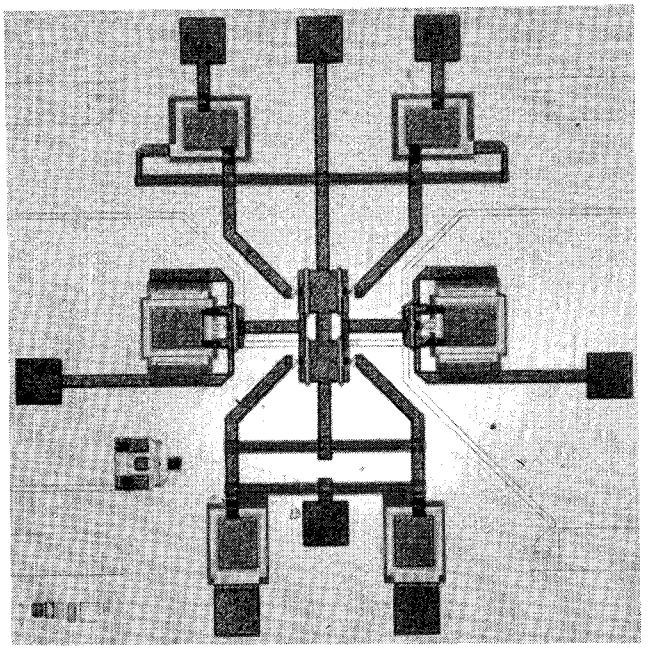

Figure 3. Monolithic Modulator

The audio offset frequency applied to each pair is 1000 Hz, and the voltage of this signal is such that the FET is driven between saturation and pinch-off. The measured performance of the prototype is shown in Figure 4 for 2 GHz carrier and in Figure 5 for a 7 GHz carrier. The conversion loss at 2 GHz is 20 dB and the suppression of the carrier is 22 dB. With a 7 GHz carrier the conversion loss is approximately 16 dB and the suppression of spectral products, including carrier, undesired sideband, and third harmonic, is 17 dB or more.

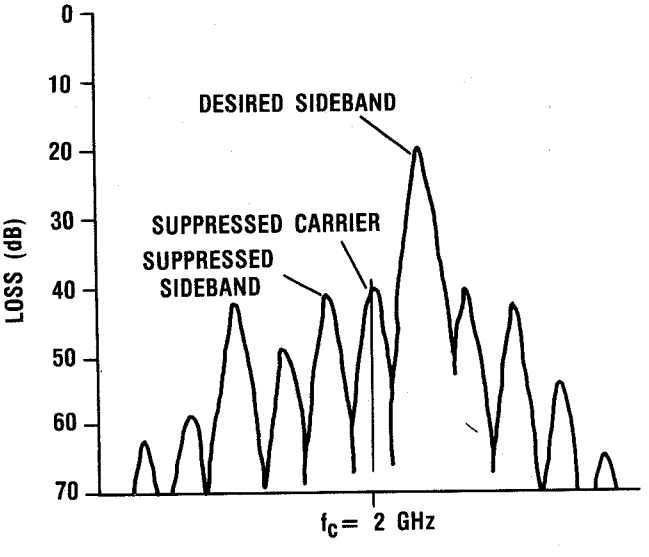

Figure 4. Monolithic Modulator Performance With F_c = 2 GHz and F_m = 10 KHz

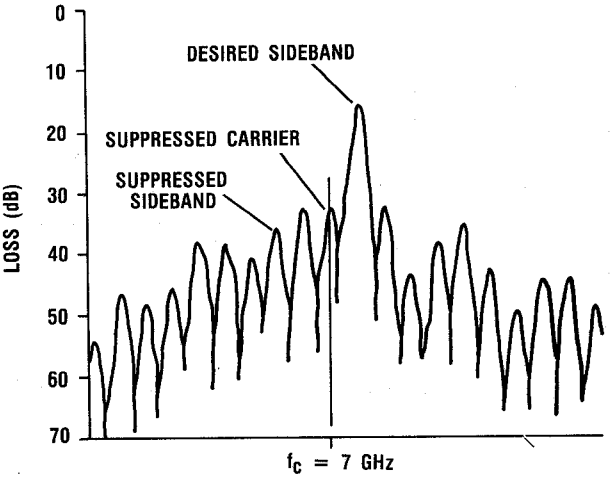

Figure 5. Monolithic Modulator Performance With F_c = 7 GHz and F_m = 500 Hz

ANALYSIS

The prototype monolithic modulator was used to verify a PSPICE model. The FET model parameters were obtained by curve fitting measured FET I-V characteristics with PSPICE calculated curves. PSPICE predictions of monolithic modulator performance were compared to measured results at 2 GHz as a function of device bias conditions and input signal levels. The PSPICE Fourier analysis routine was performed with the carrier frequency at 2 GHz. PSPICE will provide information on 8 harmonics, so in order to see the relative levels of the modulation, carrier and two sidebands, the modulation frequency is selected to be 250 MHz. In Tables 1,2, and 3, carrier suppression as a function of audio voltage and bias conditions measured on the 150 μm modulator are compared to PSPICE predictions. The model accurately predicts the optimum bias conditions for carrier suppression. The model is used to predict conversion loss of an unmatched modulator as a function of frequency in Table 4. The model may also be used to predict undesired sideband rejection as a function of coupler performance and FET balance. In Table 5, undesired sideband suppression as a function of audio quadrature quality is compared to measured results.

TABLE 1. Carrier Suppression As A Function Of Audio Signal A.C. Voltage
V_D = 6V, V_G = 3.5V

Audio Signal (volts)	Carrier Suppression	
	Predicted (dB)	Measured (dB)
2.0	15	13
2.5	22	22
3.0	18	15
3.5	14	4

TABLE 2. Carrier Suppression As A Function Of Drain Voltage
V_G = 3.5V

Drain Voltage (volts)	Carrier Suppression	
	Predicted (dB)	Measured (dB)
5.0	6	9
6.0	22	22
7.0	11	11
8.0	4	4

TABLE 3. Carrier Suppression As A Function Of Gate Voltage
V_D = 6V

Gate Voltage (volts)	Carrier Suppression	
	Predicted (dB)	Measured (dB)
3.0	10	12
3.5	22	22
4.0	8	11

TABLE 4. Conversion Loss As A Function OF Frequency

Frequency (GHz)	Conversion Loss	
	Predicted (dB)	Measured (dB)
2	25	25
7	22	23
10	23	29

TABLE 5. Sideband Suppression As A Function Of Audio Quadrature

I - Q Phase	Sideband Suppression	
	Predicted (dB)	Measured (dB)
80°	16	19
90°	26	20
100°	30	25
110°	20	12

In Table 6 conversion loss for an unmatched modulator is predicted as FET size is increased. Increasing the size of the FETs in the differential pairs significantly improves conversion loss, however, the current source remains the same (a 150 μm) so current drain does not change. The improvement in conversion loss is a result of increased transconductance and more efficient harmonic production in the larger device, which is operating in a more nonlinear region. The conversion loss also depends on the drain to source voltage on the FET pairs. A low Vds is desirable so that the FET is operating at the knee of the I-V curve. With the larger FET, the PSPICE model predicts conversion loss as low as 8 dB with the proper bias and termination on the gates.

TABLE 6 Conversion Loss As A Function Of FET Size
Current Source is 150μm F = 7 GHz

FET Size (μm)	Conversion Loss	
	Predicted (dB)	Measured (dB)
150	22	23
300	12	-
600	8	-

CONCLUSION

A unique approach to single sideband modulation has been presented Whether implemented monolithically or with discrete FETs the technique offers significant reduction in size over conventional approaches. The approach uses GaAs MESFETs as active elements, is co-planer, and requires no baluns, thus, it is well suited for integrated monolithic circuit applications. A simple 150 μm monolithic modulator was built and tested to verify nonlinear predictions of performance, and the nonlinear analysis accurately predicts the influences of bias conditions and input signal frequency and drive level on mixer carrier suppression and conversion loss. The nonlinear analysis was used to modify circuit topology and FET size, and predicts low conversion loss (8 dB) and high carrier suppression (greater than 25 dB) in a mixer using larger FETs in the differential pairs and proper terminations on the gate and drain nodes.

REFERENCES

1) Walter R. Curtice and M. Ettenberg, "A Nonlinear GaAs FET Model For Use in The Design of Output Circuits For Power Amplifiers", IEEE Transactions of Microwave Theory and Techniques, vol MTT-33, no. 12, December 1985.

2) A. Bruce Carlson, "Communication Systems", McGraw-hill, Inc. 1975, pp. 190-200.

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